TN90001

LFPAK MOSFET thermal resistance $R_{th(j-a)}$ simulation, test and optimisation of PCB layout

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Document information

Information	Content
Keywords	LFPAK, MOSFET, thermal resistance, simulation, PCB design
Abstract	This technical note considers the thermal modeling of Nexperia LFPAK MOSFETs. Different Printed Circuit Board materials and layouts are considered.

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1 Introduction

MOSFET data sheets contain a parameter $R_{th(j-a)}$ which is the thermal resistance from junction to ambient. This is a guide to how much heat can be dissipated from the device to its surroundings in a typical application. For a surface-mounted device such as an LFPAK MOSFET this is highly dependent on the type of Printed Circuit Board (PCB) on which it is mounted. The type of PCB material, the thickness of copper and the shape of the copper footprint all contribute to $R_{th(j-a)}$.

This technical note looks at the structure of an LFPAK MOSFET and the way it is mounted on a PCB. It uses thermal modelling techniques to analyse how heat, generated inside the device, is transferred to its surroundings. Various circuit layouts are considered and tested so that developers can use an accurate value for $R_{th(j-a)}$ that closely reflects practical applications.

2 Definition of Thermal Resistance $R_{th(j-a)}$

$R_{th(j-a)}$ is the thermal resistance from working surface of the silicon crystal to the surrounding environment. It is a value that represents the net effect of all the possible series and parallel paths from the semiconductor junction to ambient and includes heat transfer by means such as conduction, convection and radiation.

$R_{th(j-a)}$ is defined as the temperature difference between junction and ambient that transfers one watt of power to the environment. It is given by:

$$R_{th(j-a)} = \frac{(T_j - T_a)}{P}$$

where:

$R_{th(j-a)}$ is measured in K/W
T_j is the junction temperature (°C)
T_a is the ambient temperature (°C)
P is the heating power dissipated inside the MOSFET (W)

3 Test method

The method used to measure $R_{th(j-a)}$ is defined by JEDEC standard 51-2A. The Device Under Test (DUT) is soldered to a FR4 test board and placed in the geometric centre of the test enclosure as shown in Figure 1 and Figure 2. The enclosure comprises a 305 mm cube made from low thermal conductivity materials such as cardboard, polycarbonate, polypropylene, wood, etc.

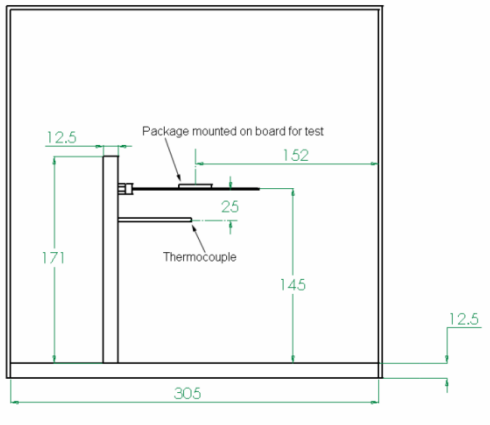


Figure 1. Test enclosure - left side view

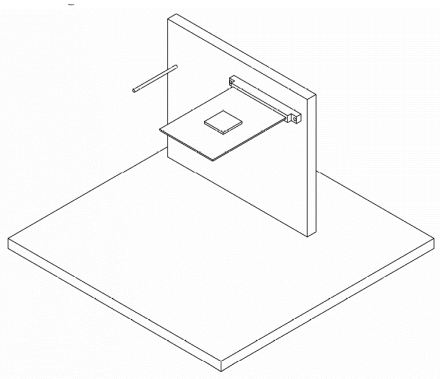


Figure 2. Isometric view of the PCB and test fixture

3.1 Heat transfer in the JEDEC enclosure

Within the JEDEC enclosure, heat is transferred from the DUT to the PCB and surroundings by three basic mechanisms; conduction, convection and radiation.

Conduction is the process by which heat transfers from high temperature parts to low temperature parts that are in contact with each other. Figure 3 shows how heat is transferred from the semiconductor junction to the copper clip and from the clip to the encapsulant. Also, from the junction through the silicon die to the mounting base, and from the mounting base to the PCB.

Convection refers to the heat transfer process caused by displacement of air surrounding the test fixture. The movement is caused by the tendency of hotter and therefore less

dense air to rise, and colder, denser air to sink under the influence of gravity, which consequently results in transfer of heat.

Radiation does not depend on contact as heat conduction and convection do. Thermal radiation is when an object loses energy in the form of electromagnetic radiation from the infrared part of the spectrum. In the example shown in Figure 3, heat is radiated from the surfaces of the MOSFET and the PCB into the space inside the box.

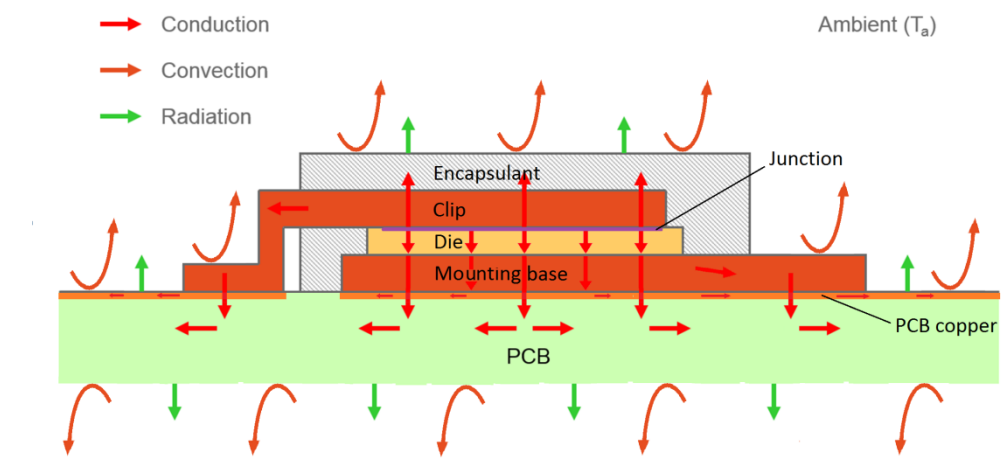


Figure 3. LFPAK MOSFET - heat transfer model

The measured thermal resistance of a MOSFET, $R_{th(j-a)}$, depends upon the package size, the material properties and the internal structure of the device. It also depends on the PCB that is used in the test fixture. Modern surface-mount MOSFETs are designed to use the PCB as a heat sink and rely on the copper traces to spread the heat over a large area to assist with cooling.

SMD Power MOSFET data sheets usually specify two values for $R_{th(j-a)}$ – one with a minimum footprint that conforms with the JEDEC standard, and another with a 25.4 mm square of 70 µm thick copper on the top surface.

Table 1. $R_{th(j-a)}$ specification in a data sheet

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-a)}$	thermal resistance from junction to ambient	Mounted on a 25.4 mm^2 square copper, 70 µm thick, FR4 1.5 mm thick PCB	-	50	-	K/W
		Mounted on a minimum footprint, 70 µm copper, FR4 1.5 mm thick PCB	-	125	-	K/W

4 MOSFET drain-source current path

Modern power MOSFETS have an ‘on’ resistance in the order of milliohms and surface-mount variants are capable of switching hundreds of Amperes. In these cases consideration must be given to the Joule heating effect of the current as it flows through the device and also the PCB traces.

Figure 4, below, shows the current path through a LFPAK MOSFET. The clip is attached directly to the semiconductor junction and at low current it acts as a heat sink, conducting heat away from the junction to the PCB. At high current, however, it becomes heated by its own resistance and requires cooling by being connected to a cooling surface connected to the source.

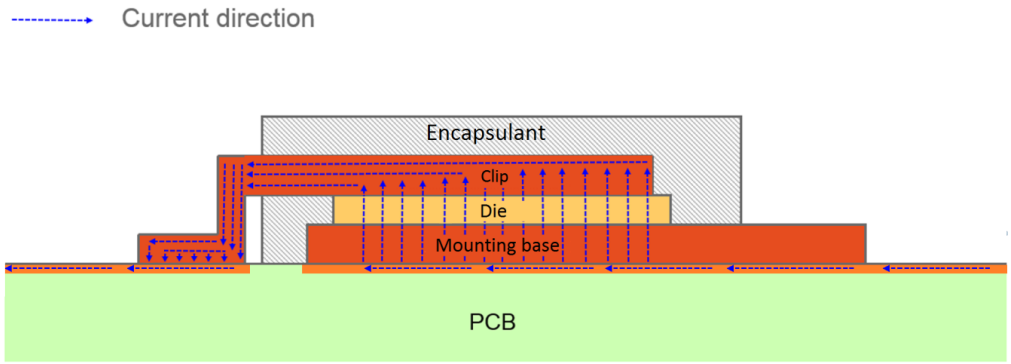
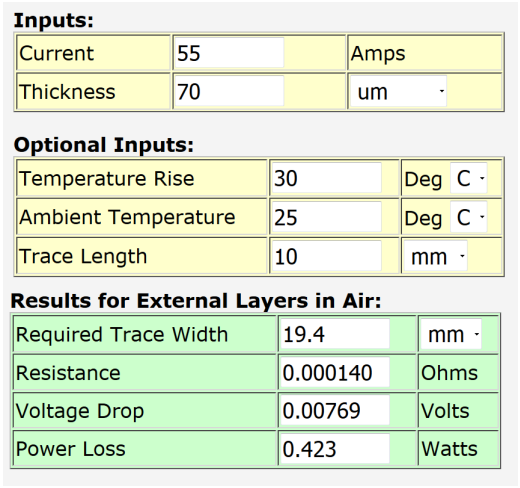


Figure 4. LFPAK package MOSFET current path shown

5 PCB trace width calculations

To examine the heating effect of the PCB trace let us consider as an example a Nexperia LFPAK MOSFET, PSMN1R0-30YLD. This has an 'on' resistance of 1 milliohm and at a typical current of 55 A the power dissipation, given by I^2R will be 55^2 x 0.001 = 3 W. This is easily dissipated by the PCB if it has a small amount of copper to spread the heat.

If we use the IPC2221 trace width calculator to work out the size of trace required to carry 55 A and allow a manageable 30 °C rise in the trace temperature, then assuming 70 µm (2 oz) thick copper, Figure 5 shows that a trace almost 20 mm wide is required.



Inputs:

Current	55	Amps
Thickness	70	um

Optional Inputs:

Temperature Rise	30	Deg C
Ambient Temperature	25	Deg C
Trace Length	10	mm

Results for External Layers in Air:

Required Trace Width	19.4	mm
Resistance	0.000140	Ohms
Voltage Drop	0.00769	Volts
Power Loss	0.423	Watts

Figure 5. IPC-2221 trace width calculator

6 Board layout optimisation

A number of thermal simulations have been carried out using a PSMN1R0-30YLD as an example to find the optimum PCB layout that extracts the maximum amount of heat from the device and therefore gives the lowest possible value for $R_{th(j-a)}$. All the simulations were on a 25.4 mm square of 70 µm thick copper. The MOSFET was fully turned on with a constant current that produced 3 W loss in the device.

The investigation examined different positions of the MOSFET within the copper square. It also considered allocating different percentages of the copper square to the source and drain. Finally, it examined the heating effect of trace width on the temperature of the MOSFET and the consequences for $R_{th(j-a)}$ measurement.

6.1 Test layout 1

In Figure 6 and Figure 7, the device is mounted on the edge of a 25.4 mm square copper pad.

$R_{th(j-a)}$ = 41.8 K/W according to the simulation result.

This layout assumes that the main heat transfer path is from the junction, through the silicon die to the mounting base. All of the copper pad is allocated to cooling the mounting base. We see from the thermal profile that very little heat reaches parts of the copper furthest away from the MOSFET and these contribute little to the cooling. The source trace is very hot because of inefficient cooling of the source pins. This is evidently not an optimum solution resulting in a relatively high value for $R_{th(j-a)}$.

Table 2. Test layout 1 and surface temperature profile

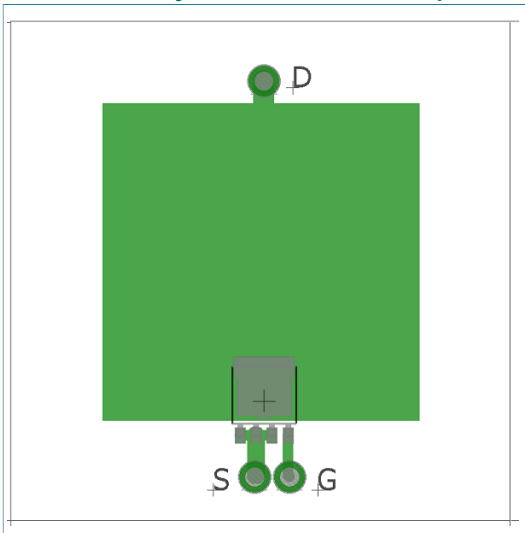


Figure 6. Test layout 1

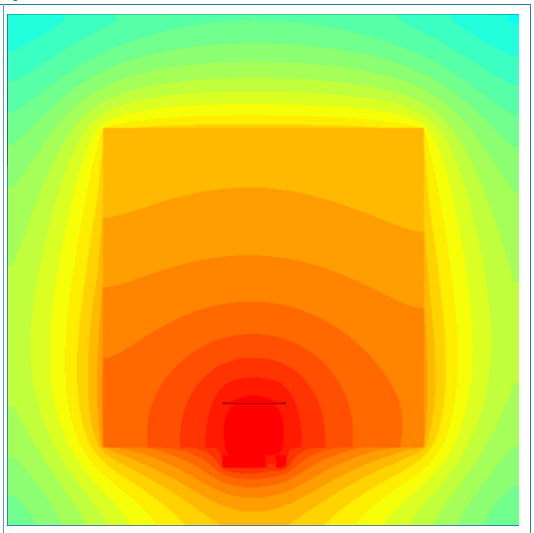


Figure 7. Surface temperature profile

6.2 Test layout 2

The test layout of Figure 8 and Figure 9 shows the MOSFET mounted in the middle of the 25.4 mm copper square with the copper area divided equally between source and drain.

The simulation result gives $R_{th(j-a)}$ = 39.1 K/W

Placing the device in the middle of the copper has improved the cooling and reduced the thermal resistance. However, the copper area connected to the drain tab is hotter than that connected to the source pins which suggest that more heat flows through the drain tab. Selecting the proper ratio of source to drain copper is important to obtain the optimum $R_{th(j-a)}$ value.

Table 3. Test layout 2 and surface temperature profile

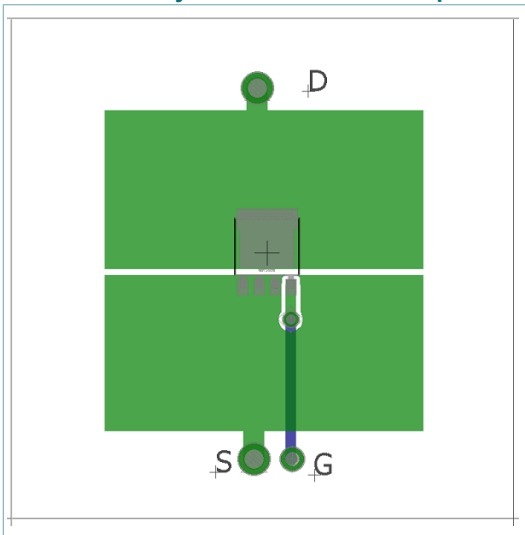


Figure 8. Test layout 2

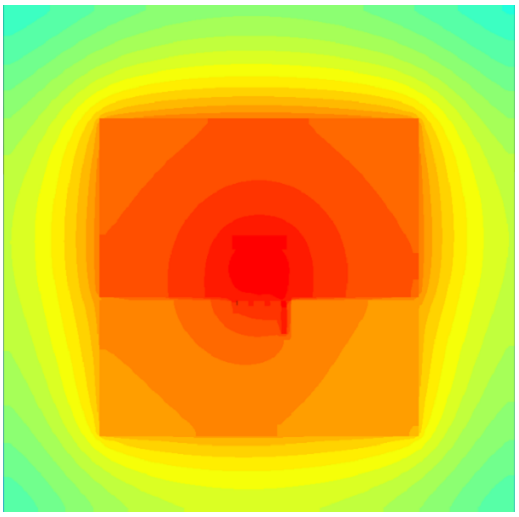


Figure 9. Surface temperature profile

6.3 Test layouts 3, 4 and 5

In Figure 10, Figure 11, Figure 12, Figure 13, Figure 14 and Figure 15 different layouts examine the effect of various trace widths for the source connection.

Layout 3 has the MOSFET located in the centre of the copper pad and the Joule heating effect of the source trace is not considered.

The simulated result gives $R_{th(j-a)}$ = 38.6 K/W

Table 4. Test layout 3 and surface temperature profile

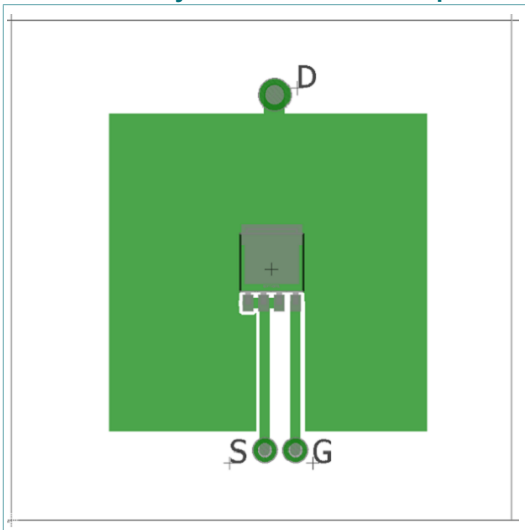


Figure 10. Test layout 3

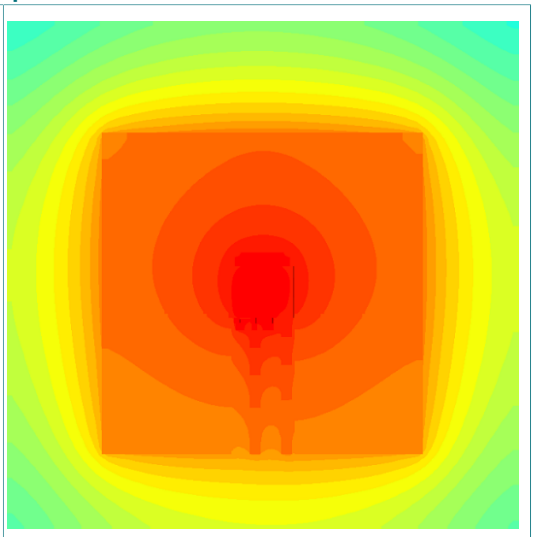


Figure 11. Surface temperature profile

But in a practical working circuit when low R_{DSon} MOSFETs are fitted, the drain-source current can reach tens or even hundreds of Amperes, and the heat generated in the PCB traces cannot be neglected.

Test layout 4 shows what happens when the Joule heating of the source trace is taken into account. In this case the trace width is 0.8 mm. The power loss in the MOSFET is 3 W as before, but the power loss in the trace is 8.8 W. Figure 13 shows the rise in temperature of the source trace which is higher than the die temperature of the MOSFET and is therefore heated significantly.

The simulated $R_{th(j-a)}$ is 92.4 K/W

Table 5. Test layout 4 and surface temperature profile

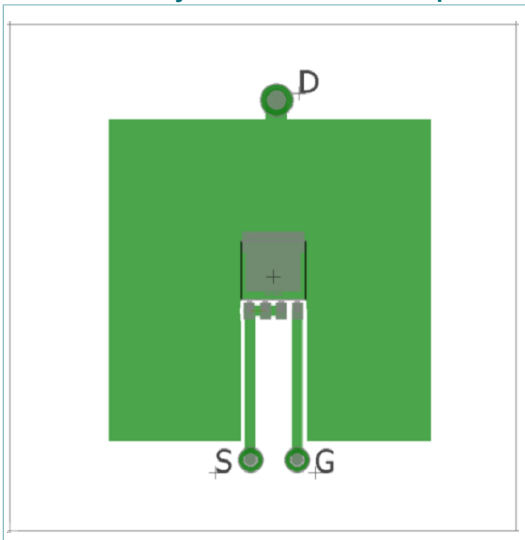


Figure 12. Test layout 4

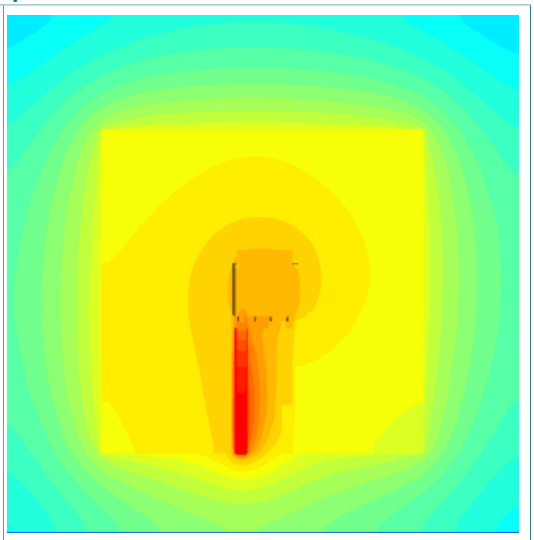


Figure 13. Surface temperature profile

Test layout 5 has the source trace increased to 3 mm. The test conditions are the same as in layout 4. This time the power loss in the source trace is reduced to 2.4 W but Figure 15 shows that the temperature still exceeds that of the die.

The simulated result for $R_{th(j-a)}$ is 56.7 K/W.

Table 6. Test layout 5 and surface temperature profile

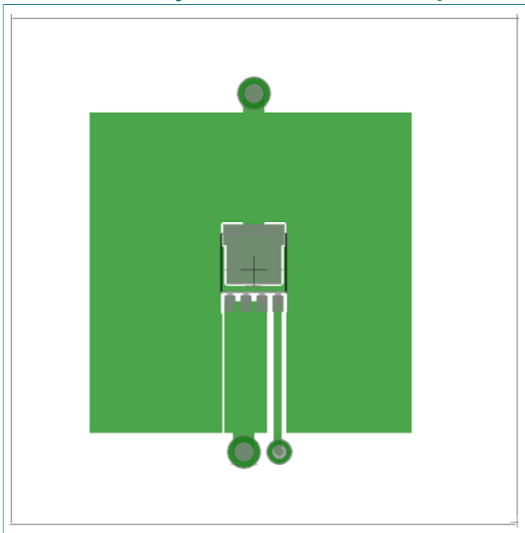


Figure 14. Test layout 5

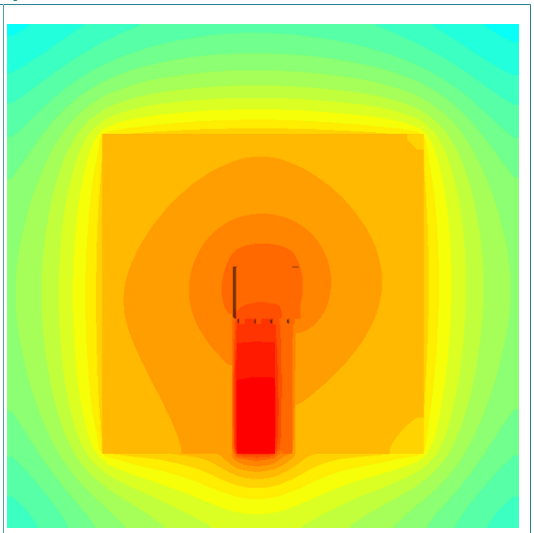


Figure 15. Surface temperature profile

We can deduce from test layouts 4 and 5 that in a practical application involving an LFPAK MOSFET careful consideration must be given to trace thickness and width so that the Joule heating of the current path does not contribute to the heating of the MOSFET.

6.4 Optimal circuit board layout 6

Test layout 6, shown in Figure 16, attempts to optimise the copper traces to obtain the lowest possible $R_{th(j-a)}$. Approximately 1/3 of the 25.4 mm copper pad is allocated to the source pins whilst the width of the source trace is a maximum.

The simulation result gives $R_{th(j-a)}$ = 37.1 K/W.

Table 7. Test layout 6 and surface temperature profile

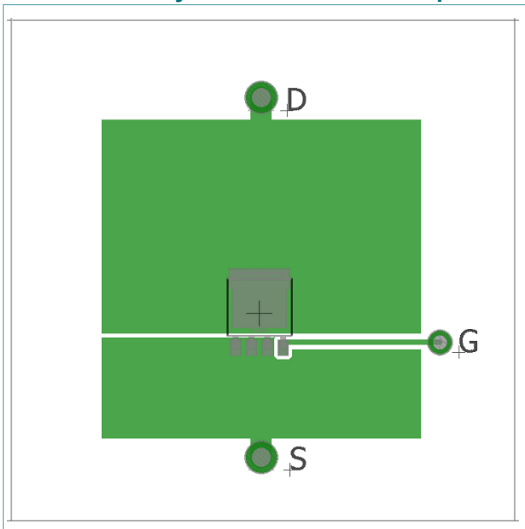


Figure 16. Test layout 6

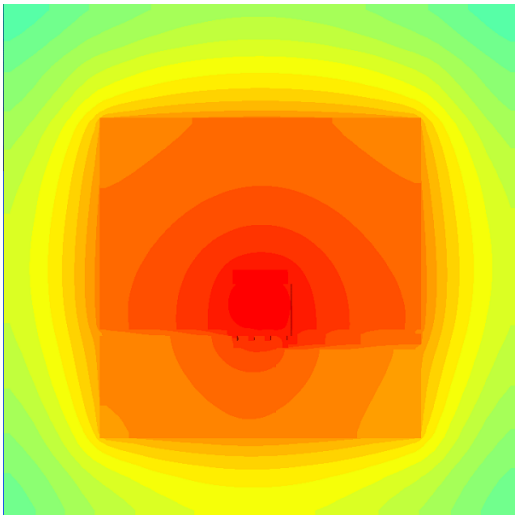


Figure 17. Surface temperature profile

7 Conclusion

LFPAK MOSFETS are designed to be soldered to a heat sink. In this case the heat sink is formed from the copper traces that make the electrical connections. This means that care must be taken in the design of the PCB and the layout of the copper traces that connect to the MOSFET. This becomes more important as the current handling capabilities of MOSFETs increases. It is now possible for a LFPAK MOSFET such as PSMN1R0-30YLD to carry 300 A and therefore not only the heat sinking properties of the copper, but the current-carrying capabilities must be taken into account by the designer.

8 Reference documents

PSMN1R0-30YLD data sheet

JEDEC 51-2A

PCB trace width calculator

9 Revision history

Table 8. Revision history

Rev	Date	Description
TN90001 v.1	20180517	Initial version

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